WHAT IS CLAIMED IS:

1. A voltage regulator circuit comprising:

a high voltage regulator capable of receiving an external high voltage supply and capable of outputting an intermediate supply voltage; and

a plurality of parallel low voltage regulators capable of receiving the intermediate supply voltage and capable of outputting a regulated output voltage,

wherein the intermediate supply voltage is no higher than a breakdown voltage of the low voltage regulators.

2. The voltage regulator circuit of claim **1**, wherein the high voltage regulator is a low dropout voltage regulator.

3. The voltage regulator circuit of claim **1**, wherein the low voltage regulators are low dropout voltage regulators.

4. The voltage regulator circuit of claim **3**, wherein the low voltage regulators have a dropout voltage of not more than approximately 14 millivolts.

5. A voltage regulator circuit comprising:

a single high voltage regulator; and

a plurality of parallel low voltage regulators capable of receiving an intermediate voltage from the high-voltage regulator, and capable of outputting a regulated output voltage,

wherein the intermediate voltage is no higher than a breakdown voltage of the low voltage regulators.

6. The voltage regulator circuit of claim **5**, wherein the high voltage regulator is a low dropout voltage regulator.

7. The voltage regulator circuit of claim **5**, wherein the low voltage regulators are low dropout voltage regulators.

8. The voltage regulator circuit of claim **7**, wherein the low voltage regulators have a dropout voltage of not more than approximately 14 millivolts.

9. The voltage regulator circuit of claim **5**, wherein each low voltage regulator comprises:

a first stage capable of receiving a reference voltage and capable of having a first current flowing through the first stage;

a second stage, coupled to the first stage, capable of having a second current flowing through the second stage; and

a third stage, coupled to the second stage, capable of outputting an output voltage and capable of having a third current flowing through the third stage,

wherein the first, second and third currents are proportional to each other throughout a range of operation of the voltage regulator between substantially zero output current and maximum output current.

10. The voltage regulator circuit of claim **9**, wherein the third stage includes a pass transistor, and the second stage includes a first mirror transistor and an input transistor in series with the first mirror transistor, and

wherein a gate of the first mirror transistor is driven by the same voltage as a gate of the pass transistor.

11. The voltage regulator circuit of claim **10**, wherein the first stage includes a second mirror transistor, wherein a gate of the second mirror transistor is driven the same voltage as the gate of the pass transistor.

12. The voltage regulator circuit of claim **11**, further including a low pass filter between the gate of the second mirror transistor and the gate of the first mirror transistor.

13. The voltage regulator circuit of claim **12**, wherein the low pass filter is an RC network.

14. The voltage regulator circuit of claim **12**, wherein the first stage includes a first trickle current source in parallel with a current source that is parallel with the first mirror transistor.

15. The voltage regulator circuit of claim **14**, further including a second trickle current source supplying a trickle current to the second stage.

16. The regulator of claim **15**, further including a first shut off transistor in series with the first mirror transistor and the input transistor of the second stage, a gate of the shut off transistor being driven by an opamp,

wherein the opamp inputs the reference voltage at a first input, and voltage from a resistor divider at a second input.

17. The voltage regulator circuit of claim **16**, further including a second shut off transistor in series with the second mirror transistor and the input transistor of the first stage, a gate of the second shut off transistor being driven by an opamp.

18. The voltage regulator circuit of claim **16**, further including an NMOS transistor between the first shut off transistor and the input transistor.

19. The voltage regulator circuit of claim **9**, wherein a phase margin of the low voltage regulator is at least 60 degrees.

20. The voltage regulator circuit of claim **9**, further including a feedback stage with a resistor divider between the third stage and the first stage, wherein a feedback voltage from the resistor divider controls an amplification of the first stage.